ABSTRACT

A method and apparatus to increase the performance of a floating point multiplier accumulator (FMAC). The method comprises receiving three floating point numbers and computing a product of the first floating point number and the second floating point number and adding a third floating point number to produce a sum value and a carry value. A propagate value, a kill value and a generate value are then computed based on the sum value and the carry value. Simultaneously the sum value is added to the carry value to create a first result, the sum value is added to the carry value and incremented by one to create a second result, the sum value is added to the carry value and incremented by two to create a third result, and a decimal point position is determined. One of the first result, the second result and the third result is then selected responsive to a rounding mode and the decimal point position. The selected result is normalized based on the decimal point position. The apparatus comprises a multiplier with a propagate, kill, generate generator (PKG generator) coupled to it. An adder, a plus-oner, a plus-two-er and a leading zero anticipator (LZA) are each coupled to the PKG generator in parallel. A rounding control unit is coupled to the LZA and coupled to a multiplexor that outputs a result from one of the adder, the plus-oner, and the plus-two-er responsive to the rounding control unit. A normalization shifter is coupled to the multiplexor and the LZA.